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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,313	05/09/2001	Tatsuya Usami	NEC01P069-MSb	2820

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	
MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/851,313	USAMI, TATSUYA	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 04/19/07

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,4,5,8,31,34,35,37,38,40-53,55,56 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4,5,8,31,34,35,37,38,40-53,55,56 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The rejection under USC §112, second paragraph is withdrawn in view of the applicants' amendments filed 04/19/2007.

2. The cancellation of claims 2, 3, 6, 7, 9-30, 32, 33, 36, 39 and 54 is acknowledged.

3. Claims 1, 4, 5, 8, 31, 34, 35, 37, 38, 40-53, 55 and 56 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 5, 8, 31, 34, 35, 37, 38, 40-53, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yau et al. (U.S. 6,054,379, hereinafter Yau) in view of Allada et al. (6,218,317 B1, hereinafter Allada) and the Applicants' Admitted Prior Art (hereinafter the prior art).

In reference to claims 1, 5, 40-42, 46, 48, 49, 52 and 55, Yau (Fig.10H) teaches a multilayered dielectric stack comprising a first insulation layer (710) comprising an polymeric organic material having a dielectric constant which is lower than a silicon oxide dielectric constant; a second insulation layer (714) made of a polysiloxane compound having an Si-H group and formed on and adhering to a top of said first insulation layer (710); a third insulation layer (716) comprising an inorganic material and

formed on and adhering to a top of said second insulation layer (714); and a plurality of wires (724) which are formed in groves formed in said multi-layered dielectric stack filling a space between said wires (724), wherein said second insulation layer (714) comprises a hydride organosiloxane which adheres to said first insulation layer (710) and said third insulation layer (716), said second insulation layer (714) improves adhesion between said first insulation layer (710) and said third insulation layer (716) (Yau, column 13, lines 12 – 663).

Yau fails to disclose wherein said second insulation layer comprises methylated hydrogen silsesquioxane film (MHSQ) at a thickness of about 50 nm, wherein said dielectric layer includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2. However, Allada (Figs.1a-1b) in a related art to the formation of copper interconnect structures teaches a second insulating film comprising a methylated hydrido organo siloxane polymer (HOSP), labeled MHSQ, wherein said polymer can be formed by spin coating processes or by conventional CVD processes (Allada, column 2, lines 7 – 67). As to the limitation that the dielectric layer includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2, the dielectric methylated hydrido organo siloxane polymer of Allada teaches upon the recited limitation. See the Response to Arguments section of this office action.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the insulating layer as taught by Allada in the interconnect formation structure of Yau, since this dielectric layers exhibit low dielectric

constants and also have better adhesion properties than conventional dielectric layers (Allada, column 1, lines 37 – 60 and column 2, lines 36-48), and furthermore, because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness (MPEP 2144.07).

The combined teachings of Yau and Allada fail to disclose wherein said MHSQ film comprises a thickness of about 50 nm. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

The combination of Yau and Allada teach wherein the first insulating layer is selected from a group including parylene, FSG, silicon oxide, or the like (Yau, column 13, lines 12 – 16) and wherein metal lines can be included on the substrate wherein said first dielectric layer covers a space between said metal lines (Yau, column 10, line

18 – column 11, line 43), but fail to disclose wherein the first insulation layer is an organopolysiloxane including methyl silsesquioxane (MSQ). However, the prior art (Instant Figs.8a-9b) teaches a device having a plurality of gate electrodes (60) having diffusion regions (54) formed on a substrate (51); and a first insulation layer (55) over said substrate (51) having a wiring connection between the gate electrodes through a diffusion region (54) locates between said gate electrodes (60), wherein said first insulation layer includes methyl silsesquioxane, and wherein said wiring connects said gate electrodes to an upper level (Instant page 2, lines 5 – 8 and page 5, lines 9 – 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yau, Allada with the teachings of the prior art to substitute the dielectric material taught by the combination of Yau and Allada for the material disclosed by the prior art because using MSQ reduces crosstalk between metal wires (Instant page 2, lines 12 – 15) and because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness. See MPEP 2144.07.

The combined teachings of the Yau, Allada and the prior art fail to expressly disclose wherein said MHSQ layer would adhere to said MSQ layer. However, this advantage would naturally flow from following the suggestion of the combination of Yau, Allada and the prior art. Therefore, Yau, Allada and the prior art inherently teach upon the claimed limitation.

In reference to claims 4 and 8, the combined teachings of Yau, Allada and the prior art teach wherein said third insulation layer comprises at least one material selected from the group including silicon oxide (Yau, column 13, lines 19 – 22).

In reference to claim 31, the combined teachings of Yau, Allada and the prior art fail to expressly teach wherein said dielectric constant of said first insulation layer is no greater than 3.5. However, the combination of Yau, Allada and the prior art teach the same material (i.e., MSQ) used for the first insulation layer (Instant page 2, lines 5 – 8 and page 5, lines 9 – 24). Therefore, the combination of Yau, Allada and the prior art inherently teach on the claimed invention.

In reference to claims 34 and 47, the combined teachings of Yau, Allada and the prior art teach wherein said first insulation layer comprises a thickness greater than a thickness of said second insulation layer; and wherein said first insulation layer can have a thickness greater than a thickness of said third insulation layer (Yau, column 13, lines 12 – 22).

In reference to claim 35, the combined teachings of Yau, Allada and the prior art further teach wherein said second insulation layers comprises more than one layer (Allada, column 2, lines 49 – 58).

In reference to claim 37, the combined teachings of Yau, Allada and the prior art teach wherein a bottom of said groove is formed on a same surface as said first insulation layer (Yau, Fig.10H).

In reference to claim 38, the combined teachings of Yau, Allada and the prior art teach wherein said plurality of wires comprises copper wires (Yau, column 13, lines 47 – 63).

In reference to claim 43, the combined teachings of Yau, Allada and the prior art teach wherein said first insulation layer, said second insulation layer and said third insulation layer of said multi-layered insulation film comprise substantially uniform widths (Yau, Fig.10H).

In reference to claim 44, the combined teachings of Yau, Allada and the prior art teach wherein a surface of said multi-layered film is substantially coplanar with a surface of said plurality of wires (Yau, Fig.10H).

In reference to claim 45, the combined teachings of Yau, Allada and the prior art teach wherein said second insulation layer is formed by plasma CVD (Yau, column 4, line 19 – column 5, line 19).

In reference to claims 50, 51 and 56, the combined teachings of Yau, Allada and the prior art teach wherein the substrate further includes a plurality of gate electrodes formed thereon; and a plurality of impurity diffusion regions formed in the semiconductor substrate, wherein said first, second and third insulation layers are formed on said plurality of gate electrodes, and wherein said plurality of grooves comprises a plurality of contact holes formed in said first, second and third insulation layers on said plurality of impurity diffusion regions and between said plurality of gate electrodes (Instant Figs.8-9, and page 4, line 1 – page 6, line 13). Further support of a multilayered dielectric stack

formed over a substrate having the recited gate electrodes and diffusion regions can be found in Lu et al. to U.S. 6,008,540 (Fig.1g and column 5, line 50 – column 6, line 67).

In reference to claim 53, the combined teachings of Yau, Allada and the prior art teach a silicon nitride layer, said first insulation layer being formed in said silicon nitride layer and said plurality of grooves having a bottom defied by an upper surface of said silicon nitride layer (Allada, column 2, lines 7 – 57).

Response to Arguments

6. Applicant's arguments filed 04/19/2007 have been fully considered but they are not persuasive.

Applicants argue, "...Yau, Allada, and the AAPA have different problems and objects to be solved, and there clearly is no motivation to combine Yau, Allada, and the AAPA as alleged by the Examiner. In short, Applicant respectfully submits that these references are unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight. In fact, Applicant submits that the references provide no motivation or suggestion to urge the combination as alleged by the Examiner. Indeed, these references clearly do not teach or suggest their combination...".

In response to this argument, Yau teaches a wiring structure including a stack of dielectric layers, wherein said stack of dielectric layers comprise three layers: a first dielectric layer selected from FSG, parylene, silicon oxide or the like (Yau, column 13, lines 12 – 16), a second layer made of an adhesive, low-k polysilioxane compound

(Yau, column 13, lines 16 - 19) and a third layer made of either silicon oxide or silicon nitride (Yau, column 13, lines 19 - 21).

Yau fails to disclose wherein said second insulation layer comprises methylated hydrogen silsesquioxane film (MHSQ) at a thickness of about 50 nm, wherein said dielectric layer includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2.

However, Allada (Figs.1a-1b) in a related art to the formation of copper interconnect structures teaches a second insulating film comprising a methylated hydrido organo siloxane polymer (HOSP), labeled MHSQ, wherein said polymer can be formed by spin coating processes or by conventional CVD processes (Allada, column 2, lines 7 – 67), resulting in a dielectric layer with low dielectric constants and better adhesion properties than conventional dielectric layers (Allada, column 1, lines 37 – 60 and column 2, lines 36-48). As to the limitation that the dielectric layer includes repeating units of $(SiCH_3O_2)_n$, $(SiO_2H)_n$ and $(SiO_3)_n$, wherein a molar ratio of $(SiO_2H)_n$ to a total of said repeating units is at least 0.2, the dielectric methylated hydrido organo siloxane polymer of Allada teaches upon the recited limitation as supported by the provided evidence, Chen et al. (Effects of slurry formulations on chemical-mechanical polishing of low dielectric constant polysiloxanes: hydrido-organo siloxane and methyl silsesquioxane).

Although Yau is open to other dielectric layers than those mentioned for the first dielectric layer, Yau fails to disclose said first dielectric layer is made of MSQ. However, the prior art (Instant Figs.8a-9b) teaches a device having a first insulation layer over

said substrate having a wiring connection between and wherein said first insulation layer includes methyl silsesquioxane (Instant page 2, lines 5 – 8 and page 5, lines 9 – 24) for the further advantage of reducing crosstalk between metal wires (Instant page 2, lines 12 – 15).

Therefore, one of ordinary skill in the art at the time the invention was made would find obvious to combine the teachings of Yau and Allada to enable substituting the polysiloxane compound in Yau with the polysiloxane compound of Allada since this dielectric layers exhibit low dielectric constants and also have better adhesion properties than conventional dielectric layers (Allada, column 1, lines 37 – 60 and column 2, lines 36-48), and furthermore, because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness (MPEP 2144.07).

Furthermore, since the first dielectric layer of Yau and Allada is open to materials other than those mentioned, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yau and Allada with the prior art to enable the dielectric material taught by Yau and Allada for the material disclosed by the prior art because using MSQ reduces crosstalk between metal wires (Instant page 2, lines 12 – 15) and because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness. See MPEP 2144.07.

However, the applicants assert that the combination of Yau, Allada and the prior art fails to expressly disclose wherein the MHSQ layer adheres to said MSQ layer and

said inorganic material. Nevertheless, this would inherent occur in the combination of Yau, Allada, and the prior art. The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
October 23, 2007

George Fourson
Primary Examiner